

FIG. 1

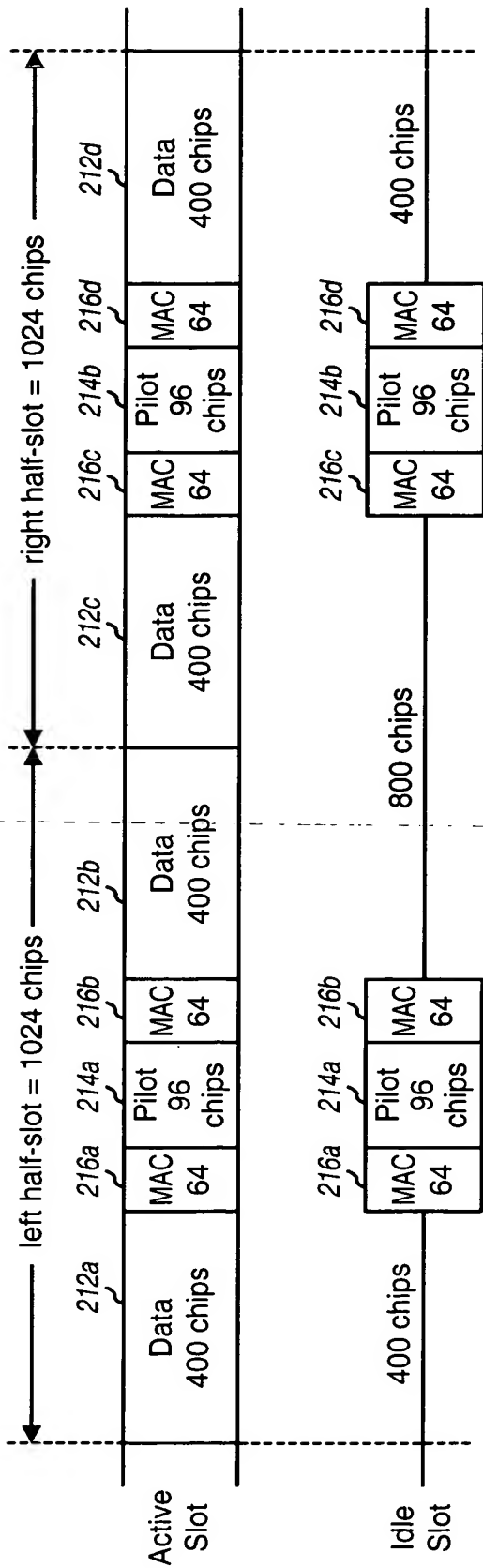


FIG. 2

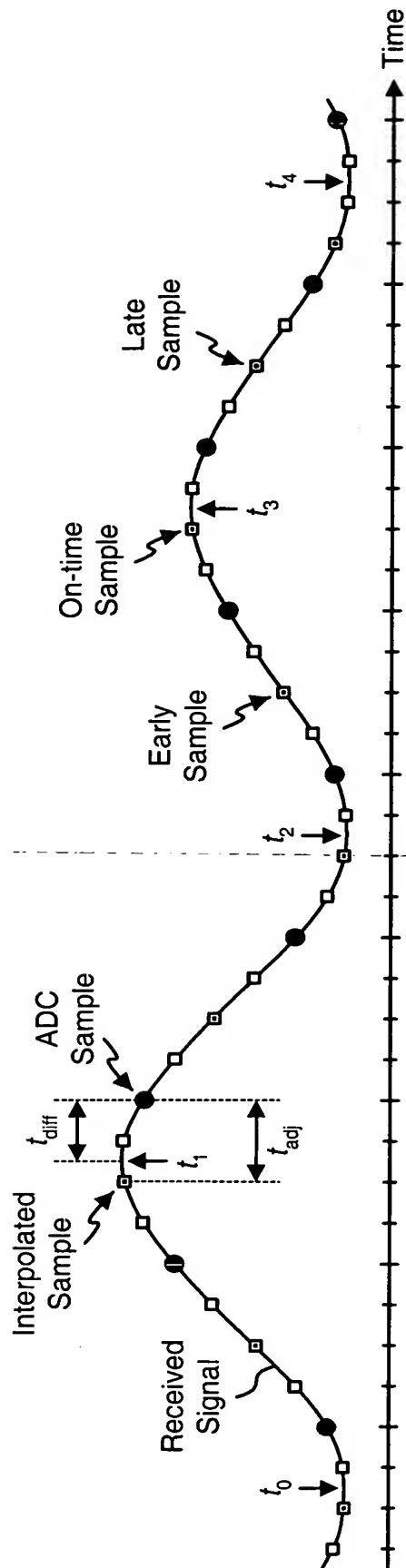
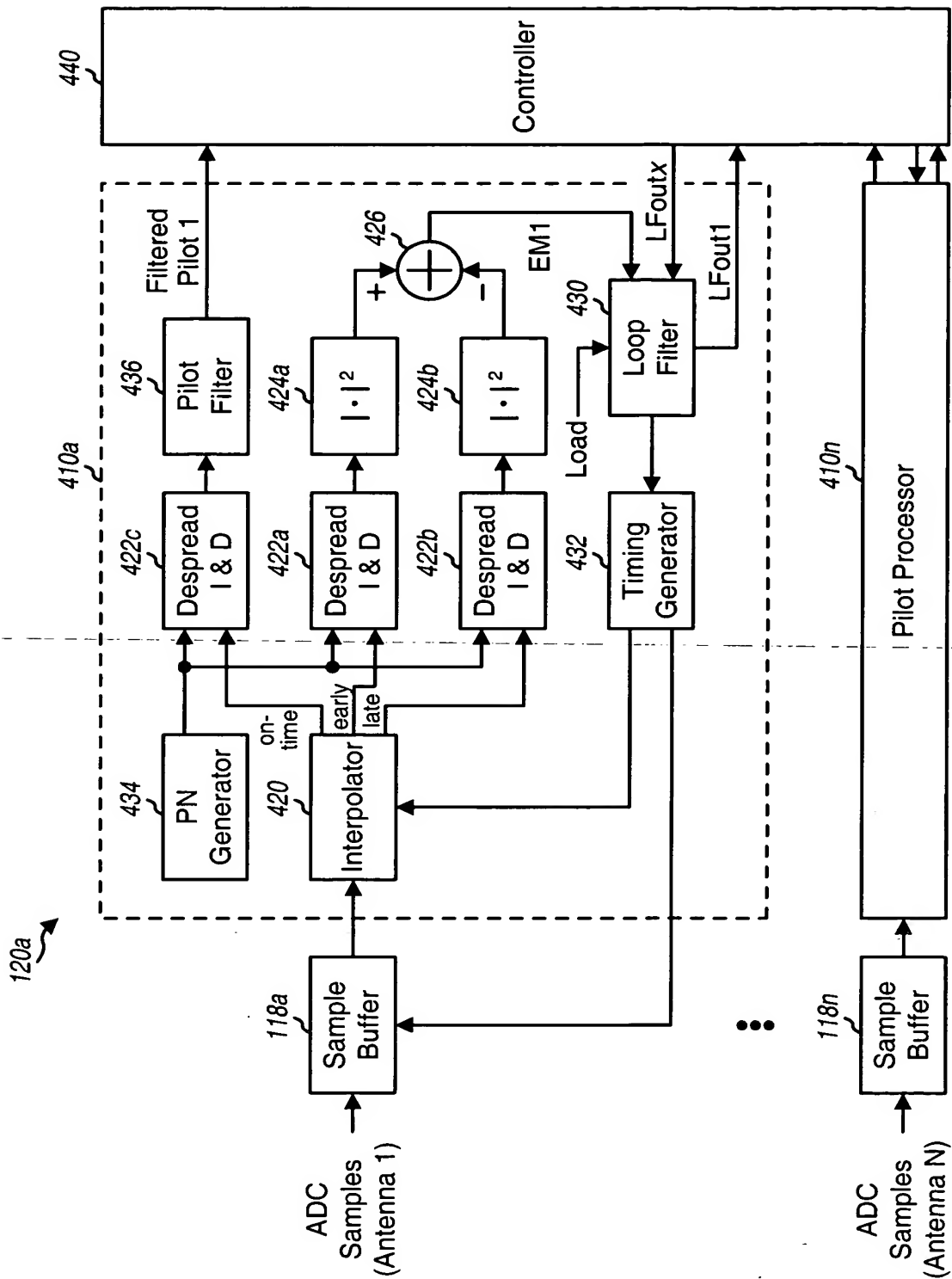


FIG. 3



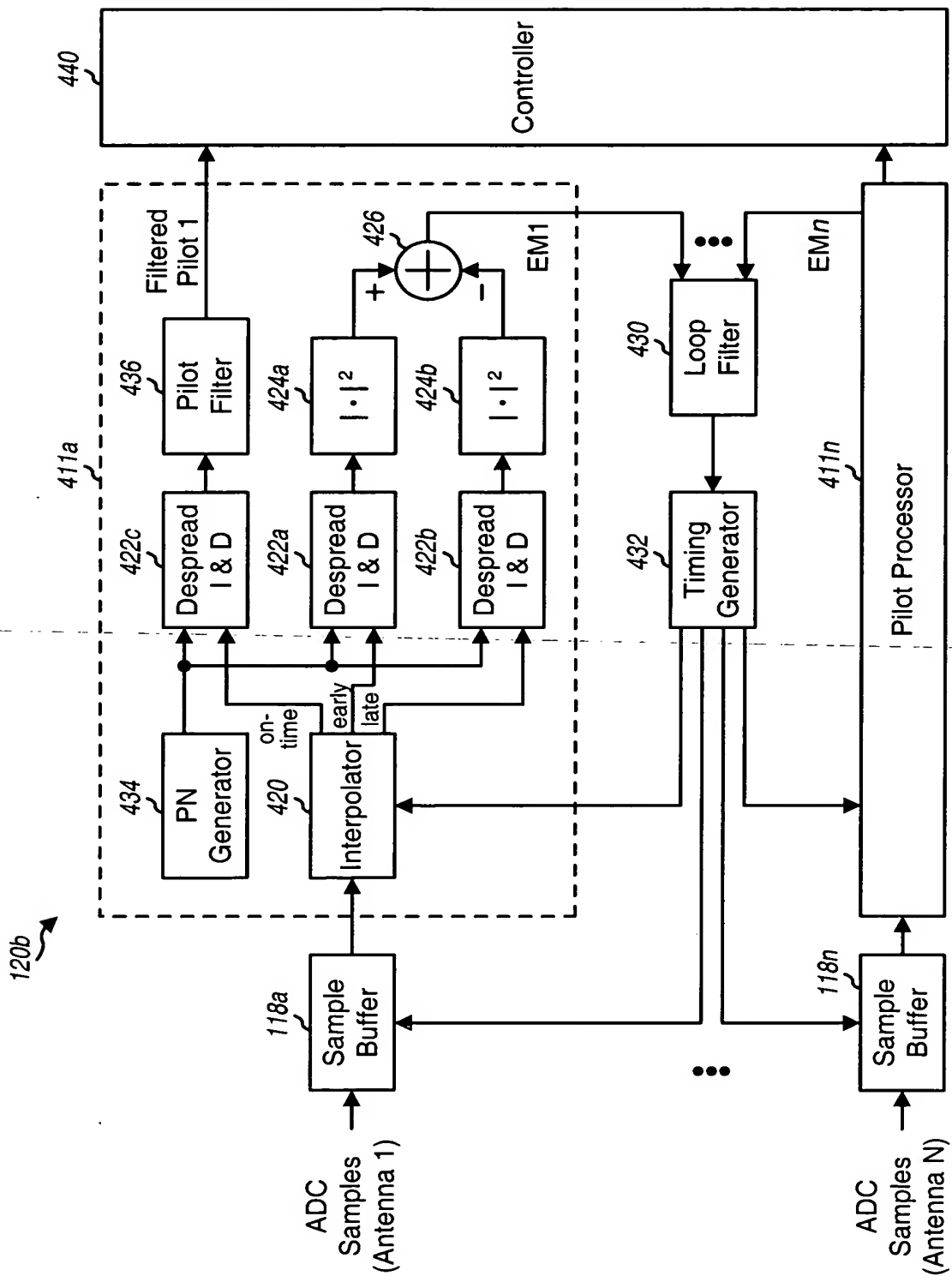


FIG. 4B

120c

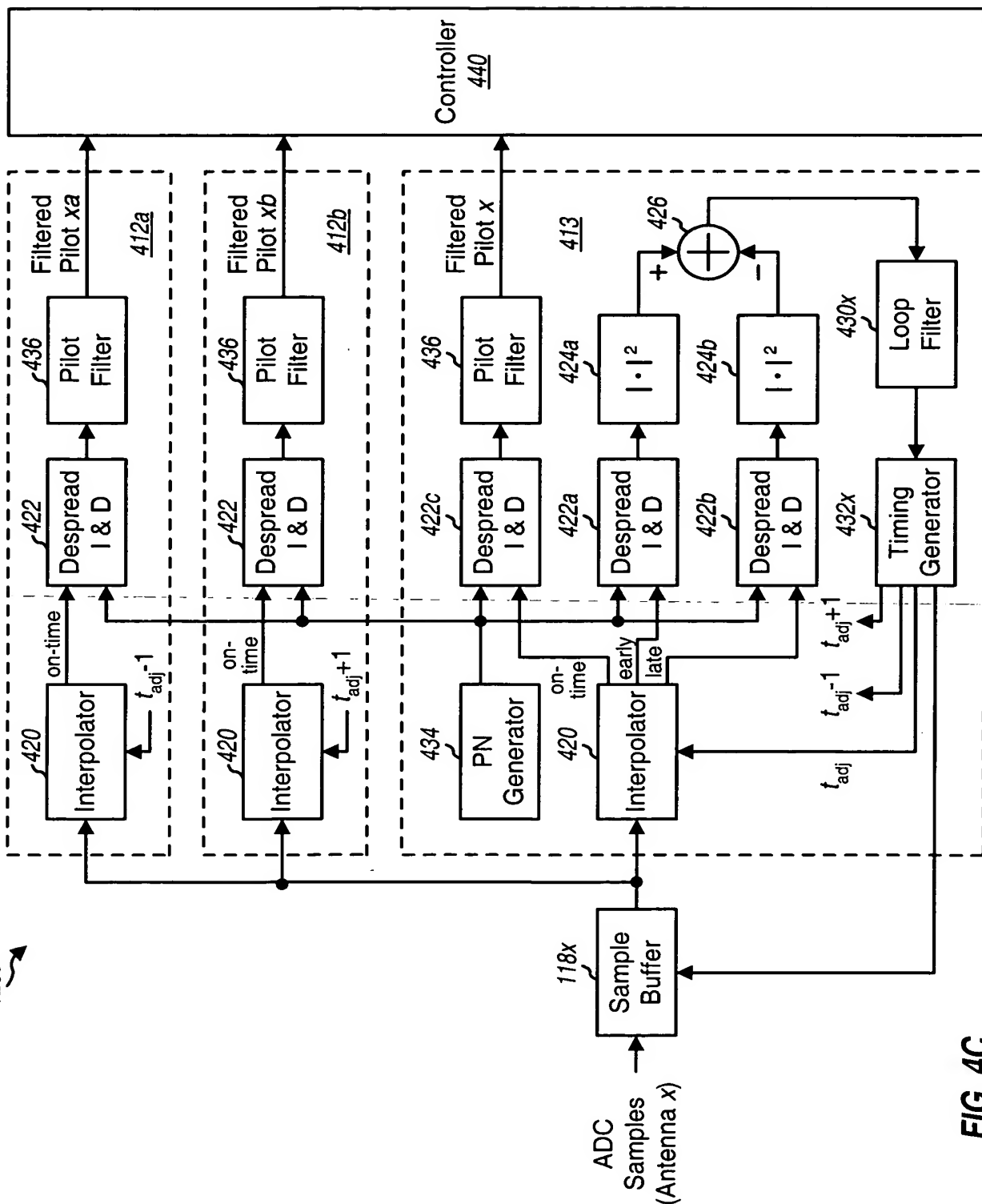


FIG. 4C

FIG. 5A is a block diagram of a first embodiment of a digital filter. The digital filter 430a includes a quantizer 532 and a register 512. The quantizer 532 receives a timing control signal and outputs a signal to the register 512. The register 512 receives a load signal and outputs a signal to a summing junction 514. The summing junction 514 also receives a signal from the loop filter input and outputs a signal to a multiplier 516. The multiplier 516 receives a gain signal  $c_1$  and outputs a signal to the summing junction 514. The output of the summing junction 514 is fed back to the quantizer 532.

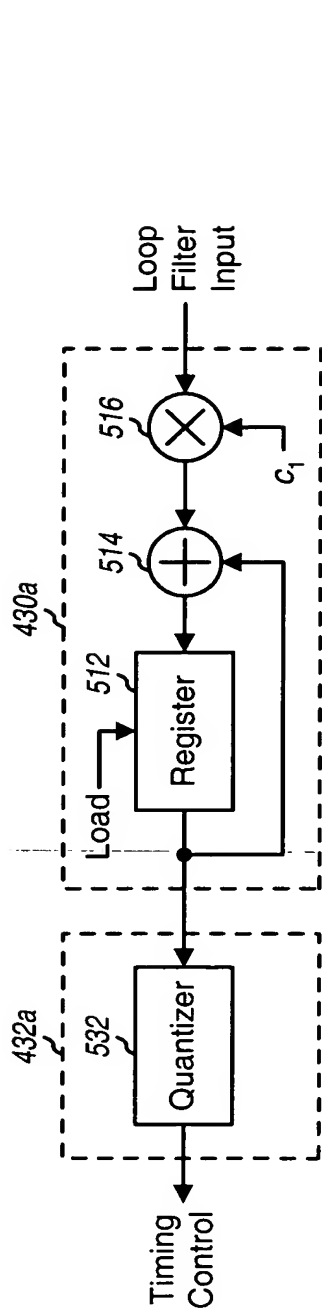


FIG. 5A

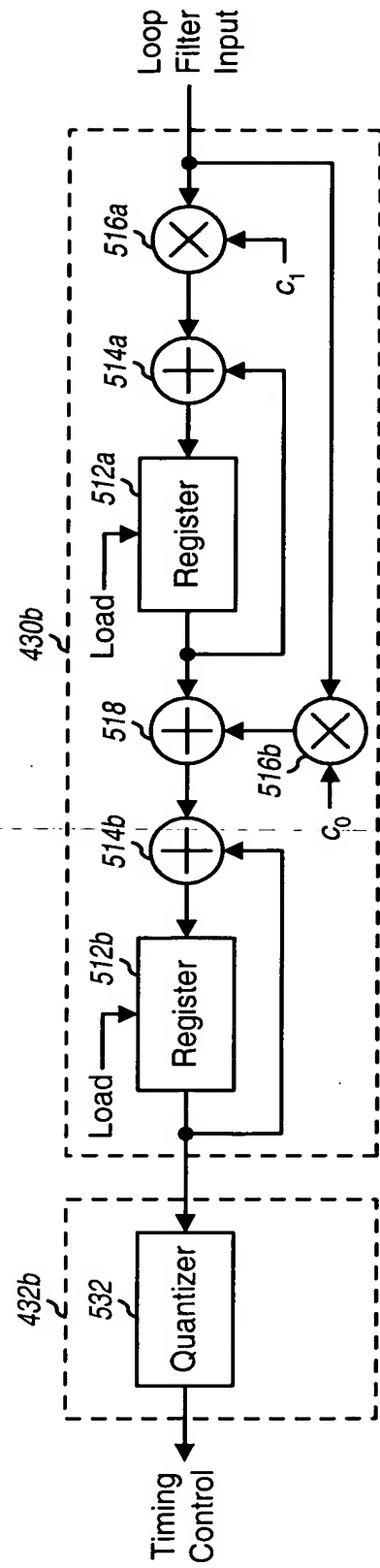


FIG. 5B

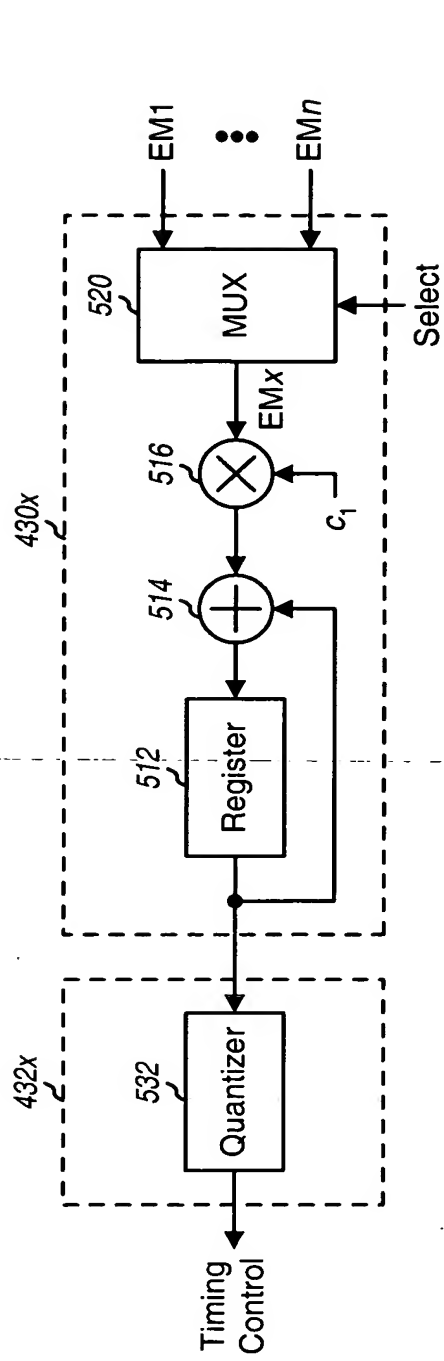


FIG. 5C

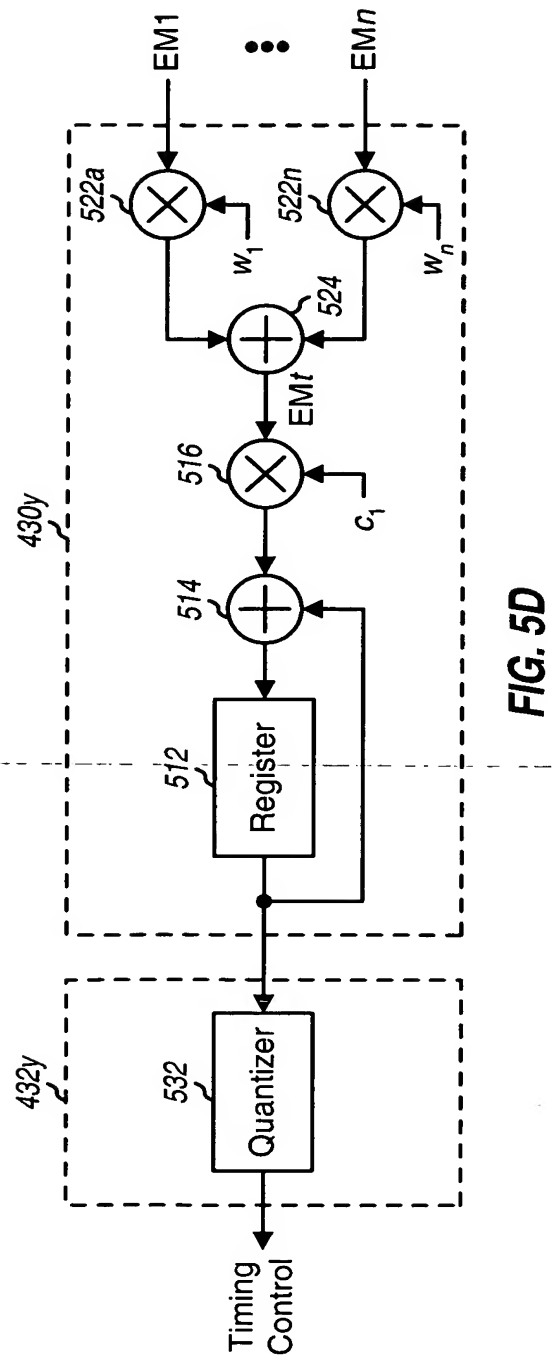
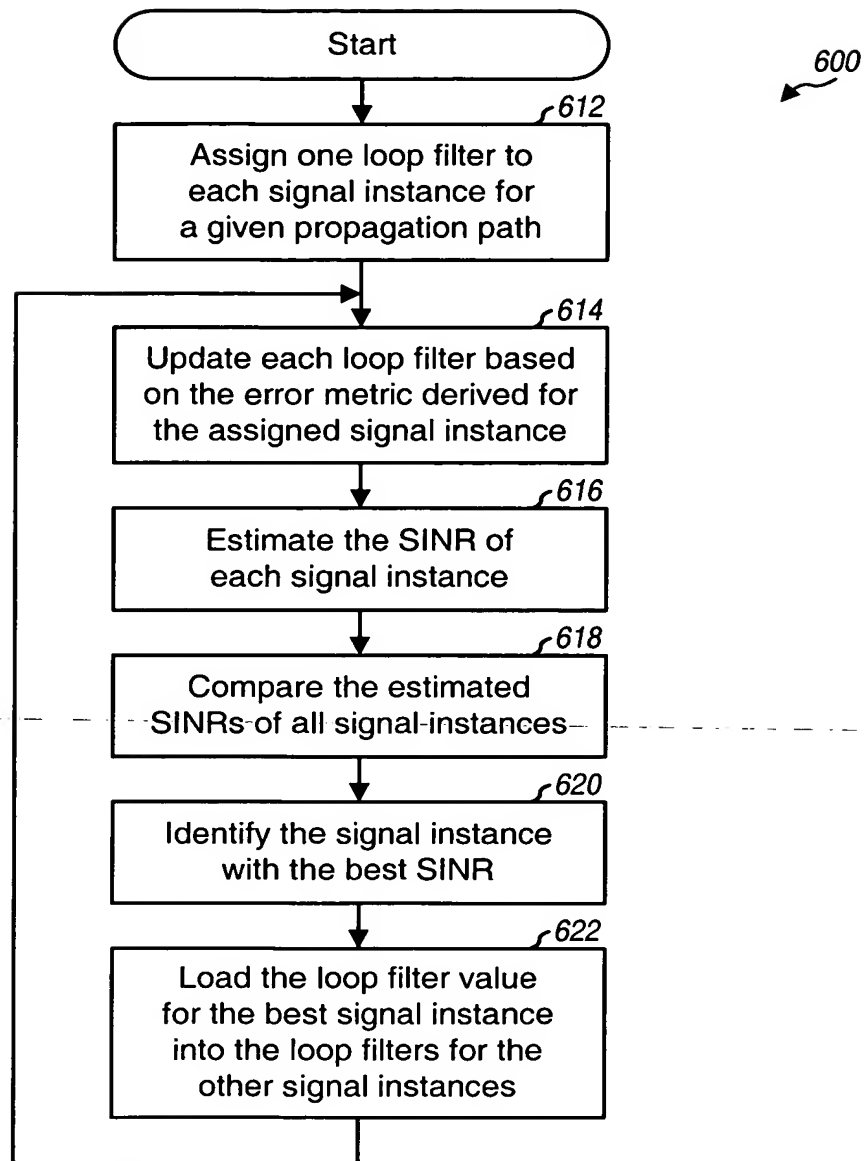
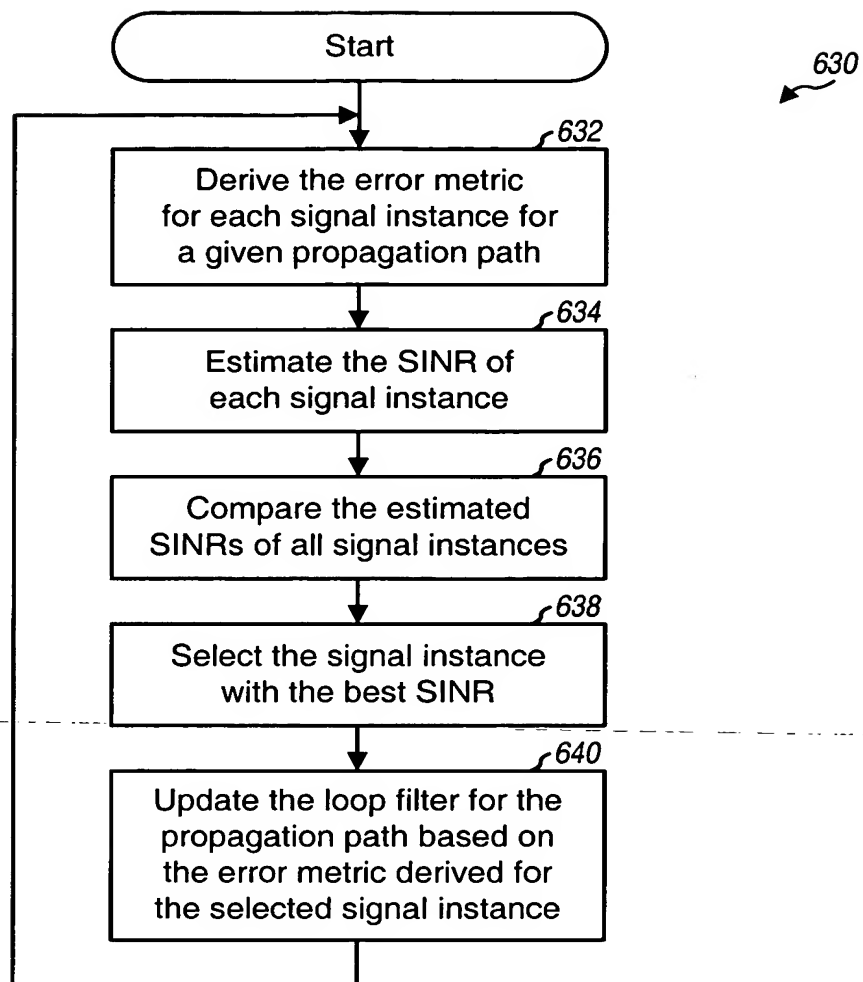


FIG. 5D

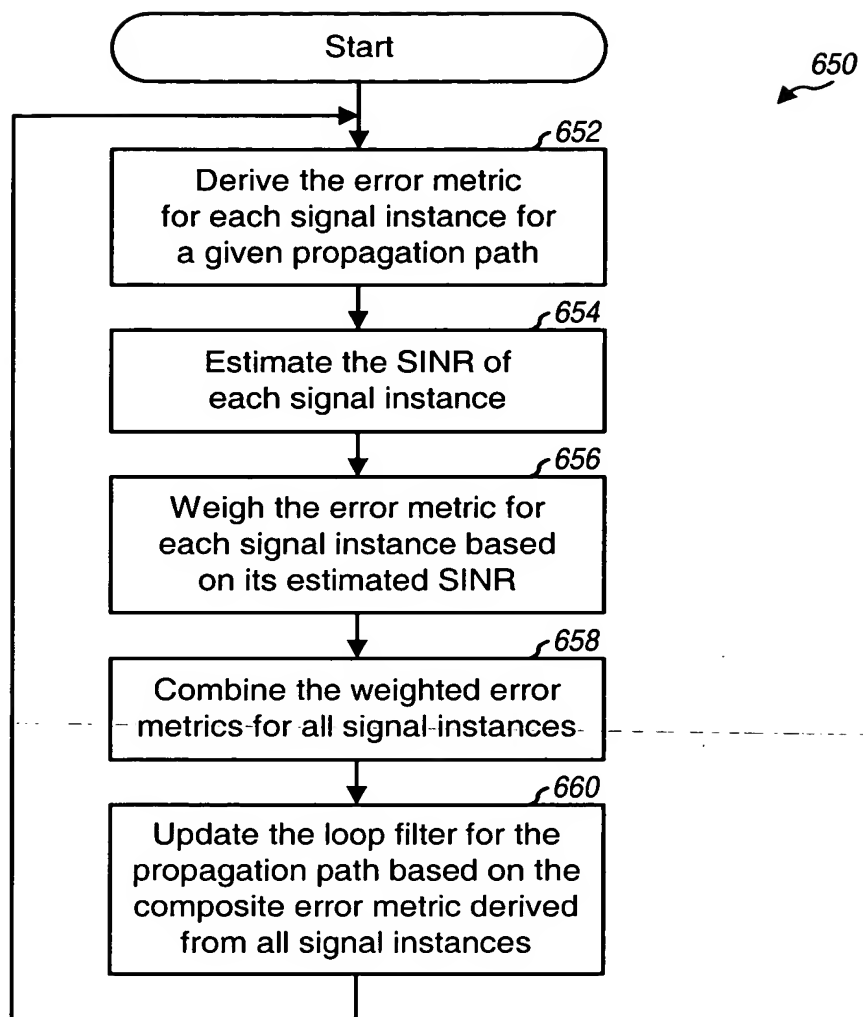


**FIG. 6A**





**FIG. 6B**



**FIG. 6C**

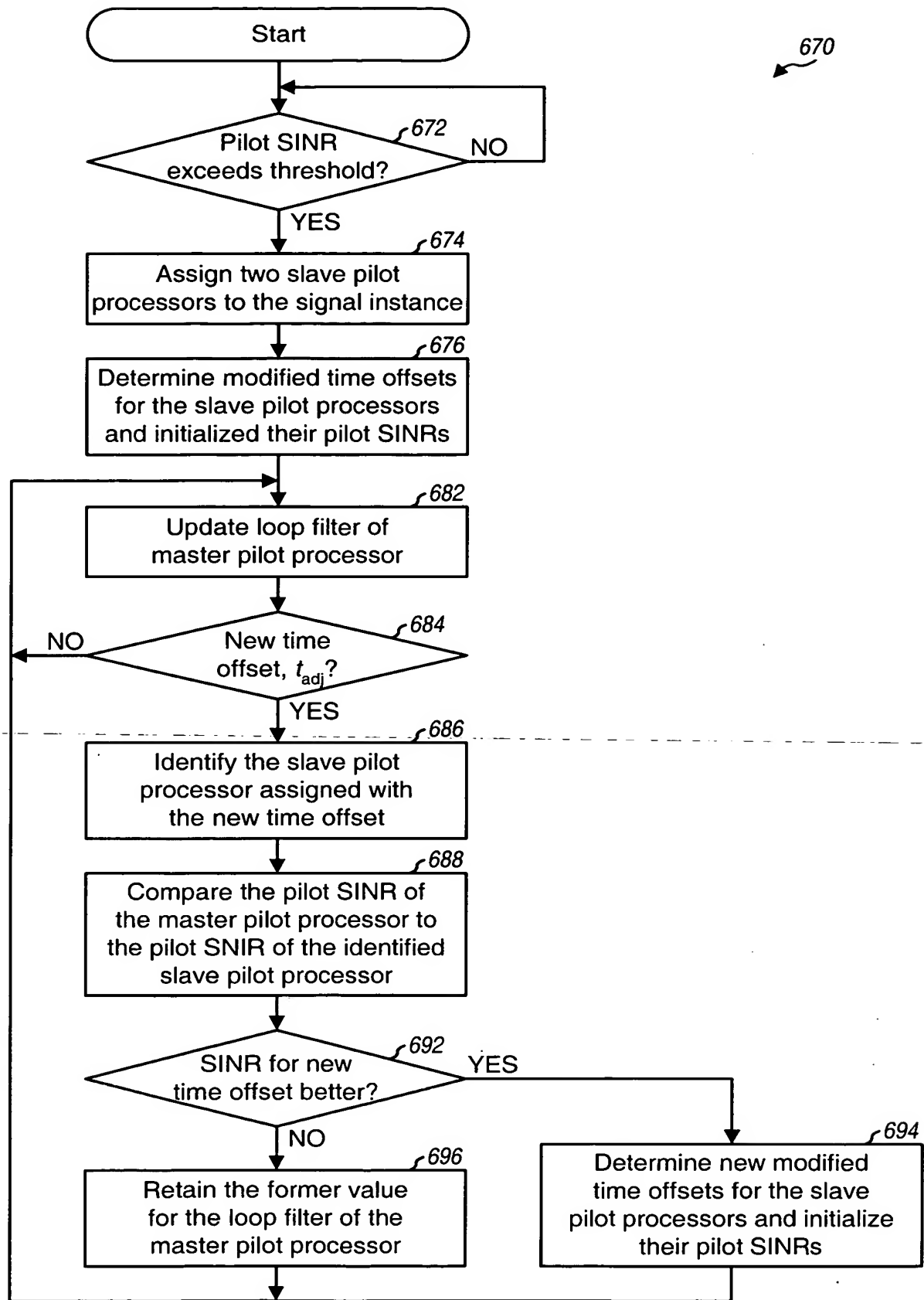


FIG. 6D